

ABSTRACT OF THE DISCLOSURE

An apparatus and method in a pipeline microprocessor are provided, for ensuring coherency of instructions within stages of the pipeline microprocessor. The apparatus includes instruction cache management logic and synchronization logic. The instruction cache management logic receives an address corresponding to a next instruction, and detects that a part of a memory page corresponding to the next instruction cannot be freely accessed without checking for coherency of the instructions within the part of the memory page and, upon detection, provides the address. The synchronization logic receives the address from the instruction cache management logic. The synchronization logic directs data cache management logic to check for coherency of the instructions within the part of the memory page, and, if the instructions are not coherent within the part of the memory page, the synchronization logic directs the pipeline microprocessor to stall a fetch of the next instruction until the stages of the pipeline